REMARKS

In response to the Office Action dated September 7, 2007, claim 1 has been cancelled, and claims 2 and 3, previously dependent from claim 1, have been rewritten in independent form. In addition, claim 3 has been amended in response to the Examiner's comments thereon.

The drawing has been amended to include reference numerals therein which correspond to the reference numerals in the specification. Finally, the specification has been amended to correct a minor error therein, so as to be consistent with the drawings.

Claims 3 and 4 stand rejected under 35 USC 102 over Tateishi, US Patent Number 5,383,177. It is respectfully submitted that these claims should be allowed thereover.

Claim 3 is set out in full:

3. A method for use in verification of a device comprising:

providing a plurality of packet classes;

providing a flag, which may be of a first or a second state, for each of the plurality of packet classes;

generating a packet;

if the flag of the packet class of the generated packet is in the first state, testing the device;

if the flag of the packet class of the generated packet is in the second state, not testing the device.

With regard to claim 3, the Examiner states:

> **For claim 3,** Tateishi teaches if the flag of the packet class of the generated packet is of the second value (see Figure 12, reference 504-506; the disposal flag is set), not testing the device (see Figure 12, 507 and 512; if disposal flag is set to 1 error rate measurement in reference 512 is not performed).

It is respectfully submitted that this is not the case.

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As stated in Tateishi as column 13, lines 43-51 (embodiment of Tateishi cited Examiner):

> In this case, even when performing the disposal of the packet data DD, the random patterns a1', b1', c1' . . . are inputted to the error detector 7 in this sequence. The error detector 7 measures an error rate of the original random patterns (step 512). Consequently, an out-of-synchronism state of the random patterns disappears.
> Thus, the error rate of the random patterns can be accurately measured even in the test involving the packet disposal.

Thus, contrary to the Examiner's statement, even if the disposal flag in Tateishi is set to 1, the error rate measurement is indeed performed. Thus, the limitations of the last paragraph of claim 3 are not met, and claim 3 is respectfully submitted to be allowable over Tateishi.

The Examiner makes the same comment with regard to claim 4. It is submitted that the last paragraph of claim 4 is not met by Tateishi in accordance with the above analysis with regard to claim 3. Claim 4 is thus also respectfully submitted to be allowable over Tateishi.

Claims 2 and 5 stand rejected under 35 USC 103 of Tateishi in view of Ramaiah et al., US Publication Number 2005/0216954. It is respectfully submitted that these claims should be allowed thereover.

Initially, it is to be pointed out that claim 5, in paragraph (d), includes a limitation similar to that in the last paragraph of claim 3. The Examiner makes the same comment as above with regard to claim 5. As pointed out above, this limitation is not disclosed by Tateishi, and thus no combination of Tateishi and Ramaiah et al. can meet the limitations of claim 5.

In regard to claim 2, it is respectfully submitted that the combination of Tateishi and Ramaiah et al. would not be obvious as suggested by the Examiner.

The Examiner states:

> The motivation for claims 2 and 5 is that one can note if the packet was in the range of allowed value. Additionally, to prevent the device under test to stop function/being able to communicate if too many packets (like the RST packets), which cause the device under test to be unable to function properly if packets (which might be generated by the random generator).

As is well understood, the Examiner must provide an apparent reason to combine the known elements in the fashion claimed and must articulate this reasoning with a rational underpinning to support a conclusion of obviousness. As stated in KSR International Co. v. Teleflex, Inc. (U.S. Supreme Court), 550 U.S.___ (2007):

> Often, it will be necessary for a court to look to interrelated teachings of multiple patents; the effects of demands known to the design community or present in the marketplace; and the background knowledge possessed by a person having ordinary skill in the art, all in order to determine whether there was an apparent reason to combine the known elements in the fashion claimed by the patent at issue. To facilitate review, this analysis should be made explicit. See *In re Kahn*, 441 F. 3d 977, 988 (CA Fed. 2006) ("R]ejections on obviousness grounds cannot be sustained by mere conclusory statements; instead, there must be some articulated reasoning with some rational underpinning to support the legal conclusion of obviousness").

The Examiner's comments provide no such "apparent reason to combine the known elements" of Tateishi and Ramaiah et al. Tateishi is concerned only with the testing of packet switching, and has no further interest suggested or disclosed in accordance with the above-quoted comments of the Examiner.

It is therefore respectfully submitted that it would not be obvious to combine the disclosures as suggested by the Examiner, and that claim 2 should be allowed.

Claim 6, dependent from claim 5, is respectfully submitted to be allowable on the basis of this dependency.

It is therefore respectfully submitted that claims 2-6 should be allowed. Reconsideration and allowance of such claims are respectfully solicited.

Respectfully submitted,

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